ABSTRACT OF THE DISCLOSURE

A transistor M1 has its drain connected to a source of a transistor M2 through a capacitor Cc_3. A series connection of a resistor R and a capacitor Cc_1 is provided between a source of the transistor M1 and a gate of the transistor M2. The transistor M1 has its gate connected to a drain of the transistor M2 through a capacitor Cc_2. Appropriate dc bias potentials P_1, P_2 and P_3 are provided for the drain of the transistor M2, the gate and the drain of the transistor M1, respectively, so that an active inductor is obtained between the gate and the source of the transistor M2.